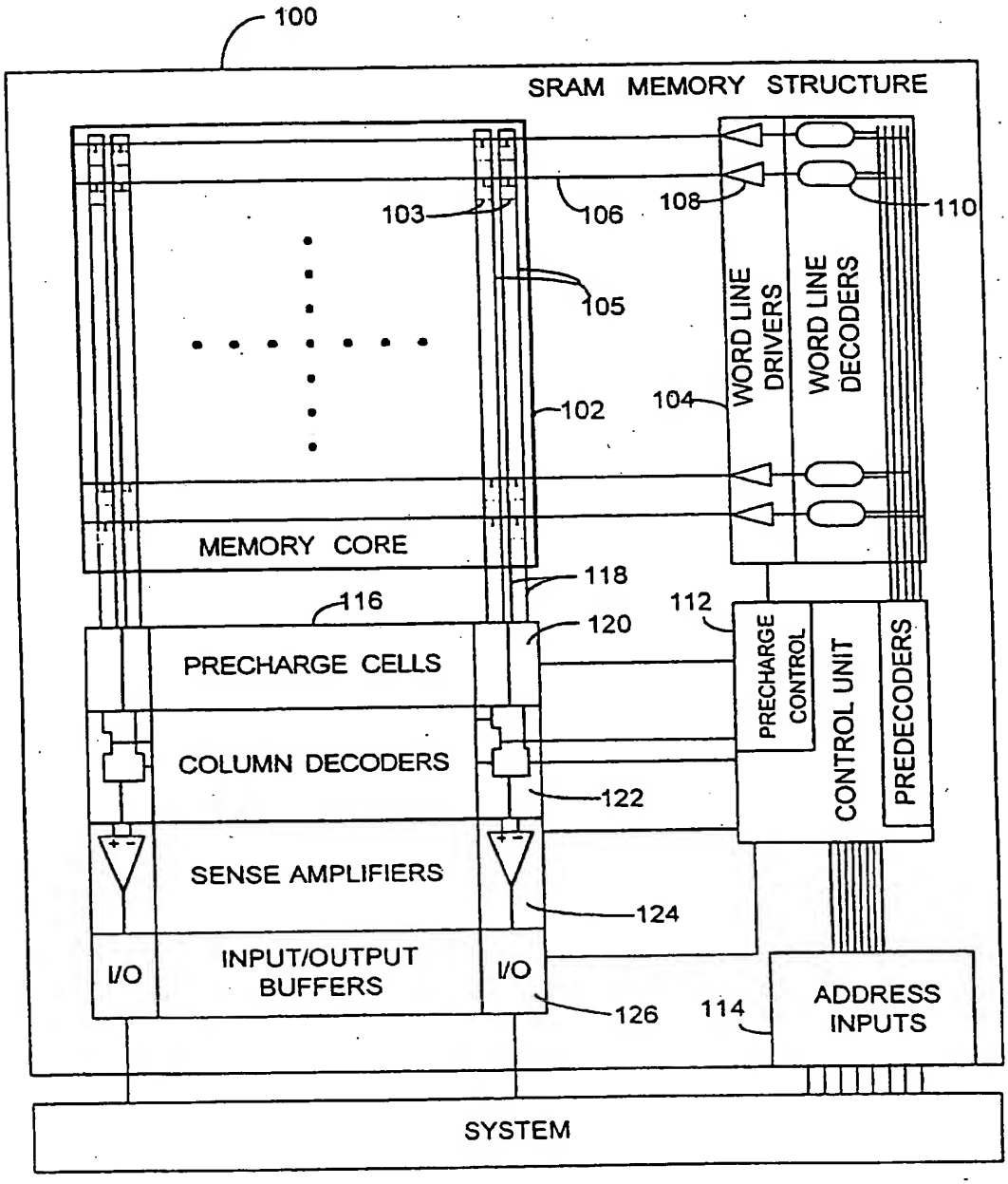
100
SRAM MEMORY STRUCTURE
103
106
108
110
105
WORD LINE DRIVERS
WORD LINE DECODERS
104
102
MEMORY CORE
118
116
112
120
PRECHARGE CELLS
PRECHARGE CONTROL
CONTROL UNIT
PREDECODERS
COLUMN DECODERS
122
SENSE AMPLIFIERS
124
I/O
INPUT/OUTPUT BUFFERS
I/O
126
114
ADDRESS INPUTS
SYSTEM

FIG. 1

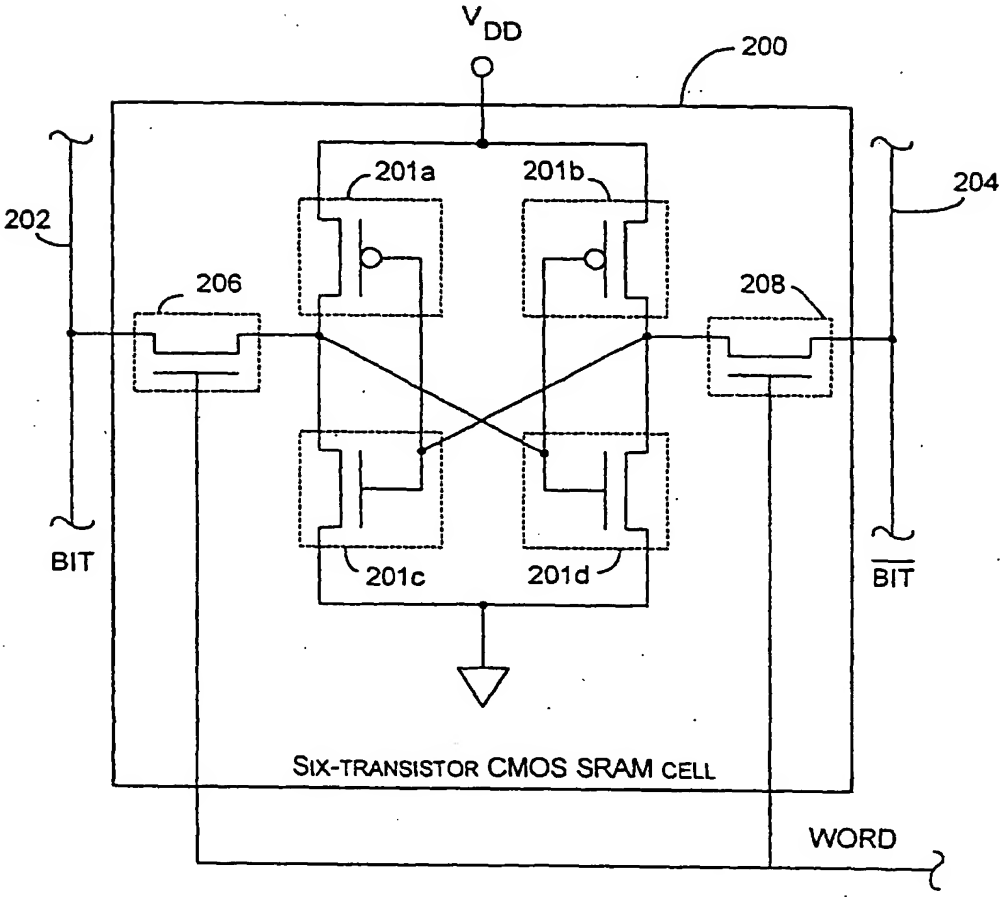
V_{DD}
200
201a
201b
202
204
206
208
BIT
$\overline{BIT}$
201c
201d
SIX-TRANSISTOR CMOS SRAM CELL
WORD

FIG. 2

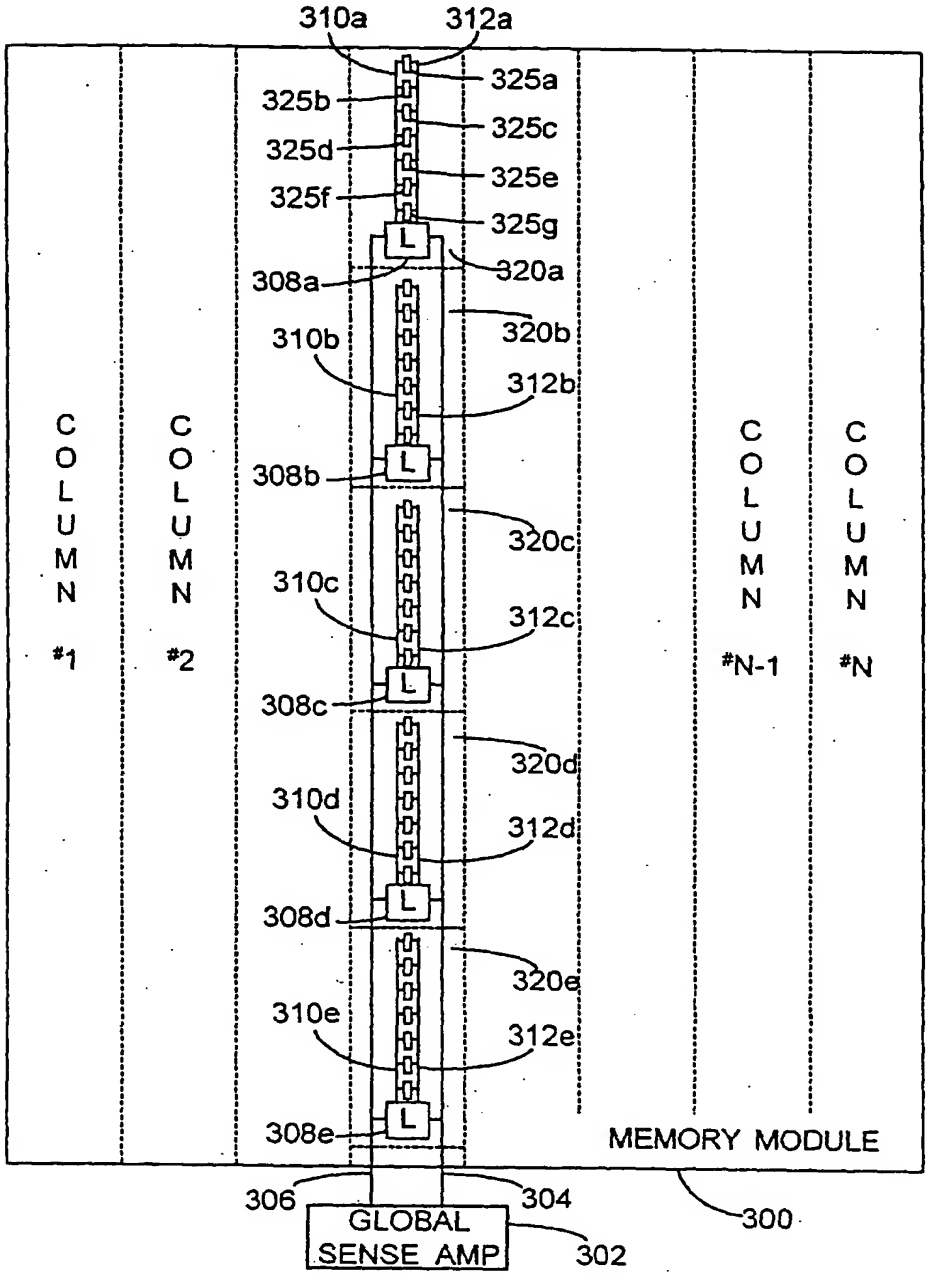
310a
312a
325a
325b
325c
325d
325e
325f
325g
L
308a
320a
320b
310b
312b
COLUMN #1
COLUMN #2
COLUMN #N-1
COLUMN #N
308b
320c
310c
312c
308c
320d
310d
312d
308d
320e
310e
312e
308e
MEMORY MODULE
306
304
GLOBAL SENSE AMP
302
300

FIG. 3

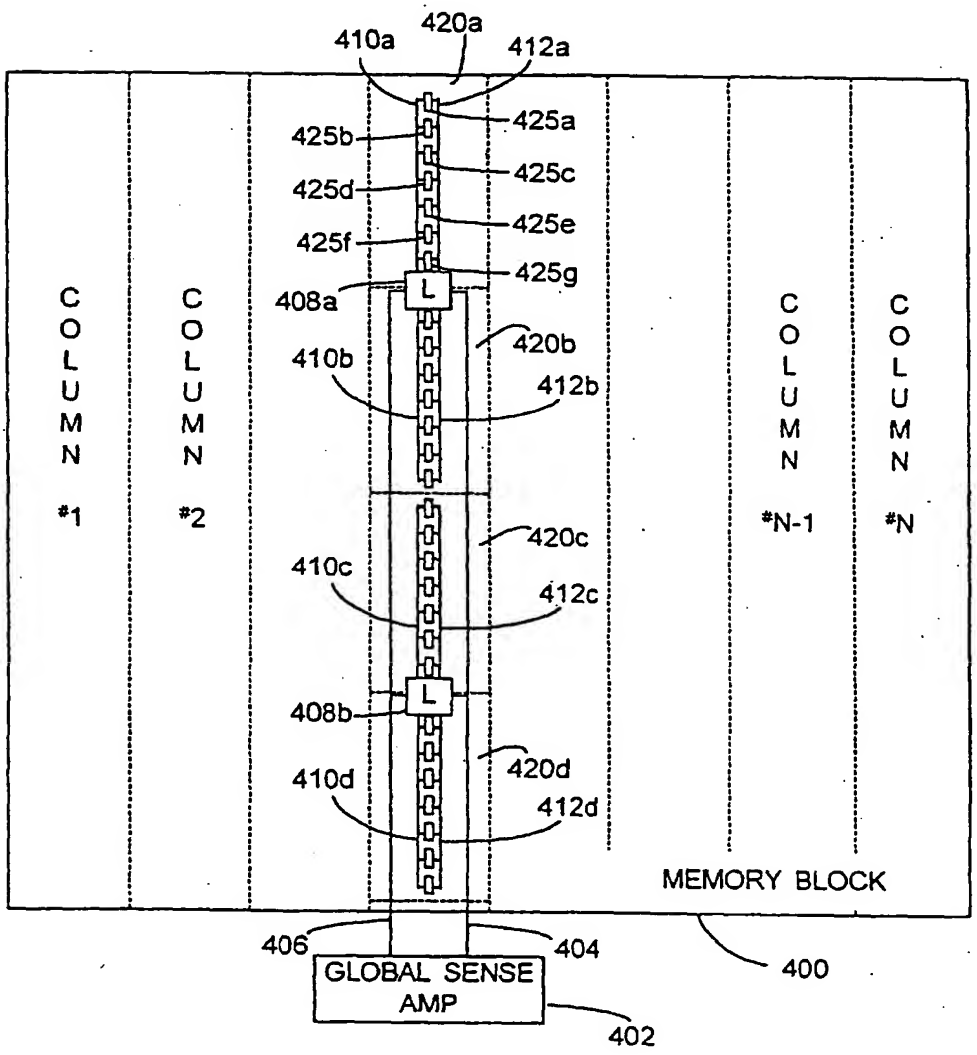
420a
410a
412a
425a
425b
425c
425d
425e
425f
425g
L
408a
420b
410b
412b
COLUMN #1
COLUMN #2
COLUMN #N-1
COLUMN #N
420c
410c
412c
L
408b
420d
410d
412d
MEMORY BLOCK
406
404
400
GLOBAL SENSE AMP
402

FIG. 4

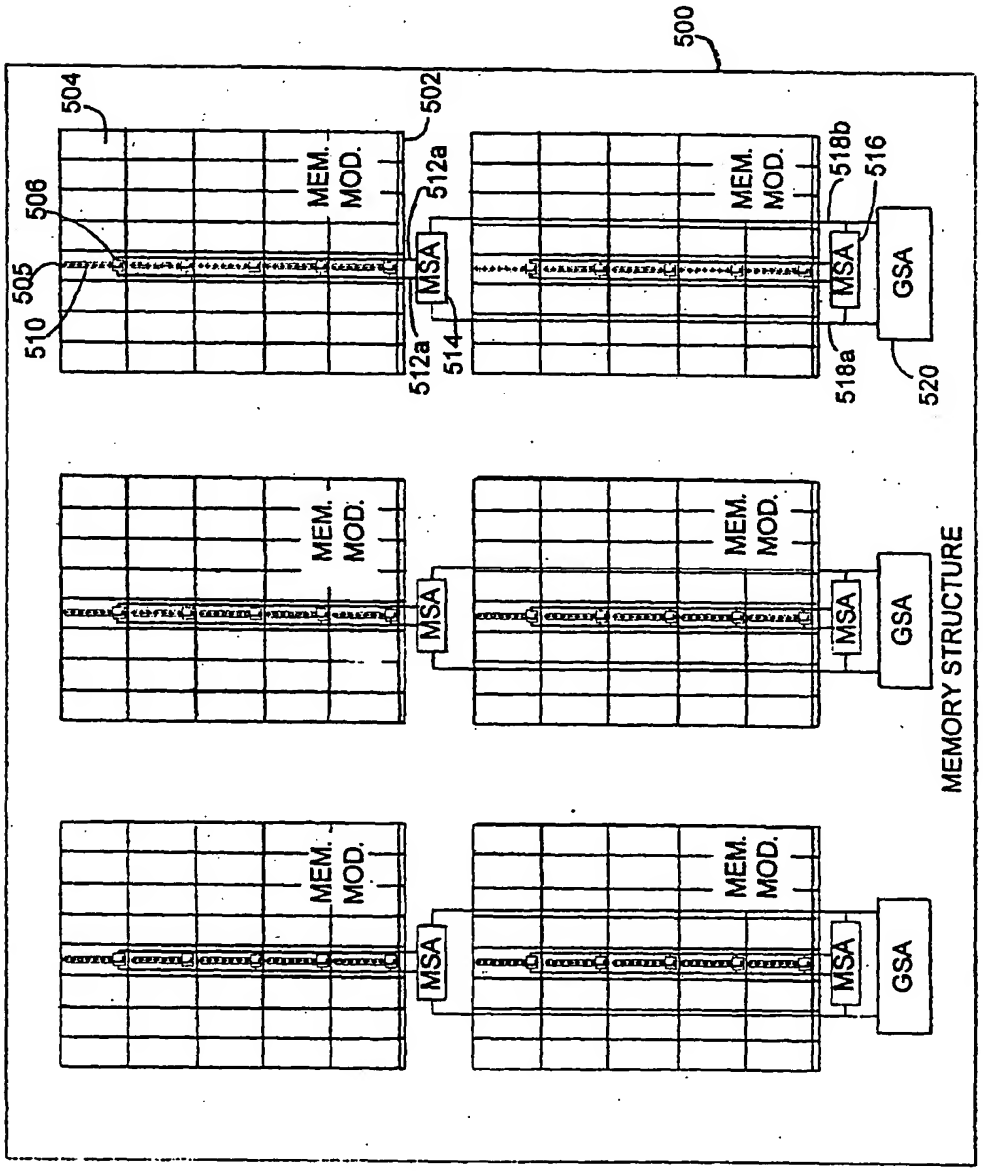
500
504
502
506
505
510
512a
MSA
514
512a
518b
516
518a
520
GSA
MEM. MOD.
MEMORY STRUCTURE

FIG. 5

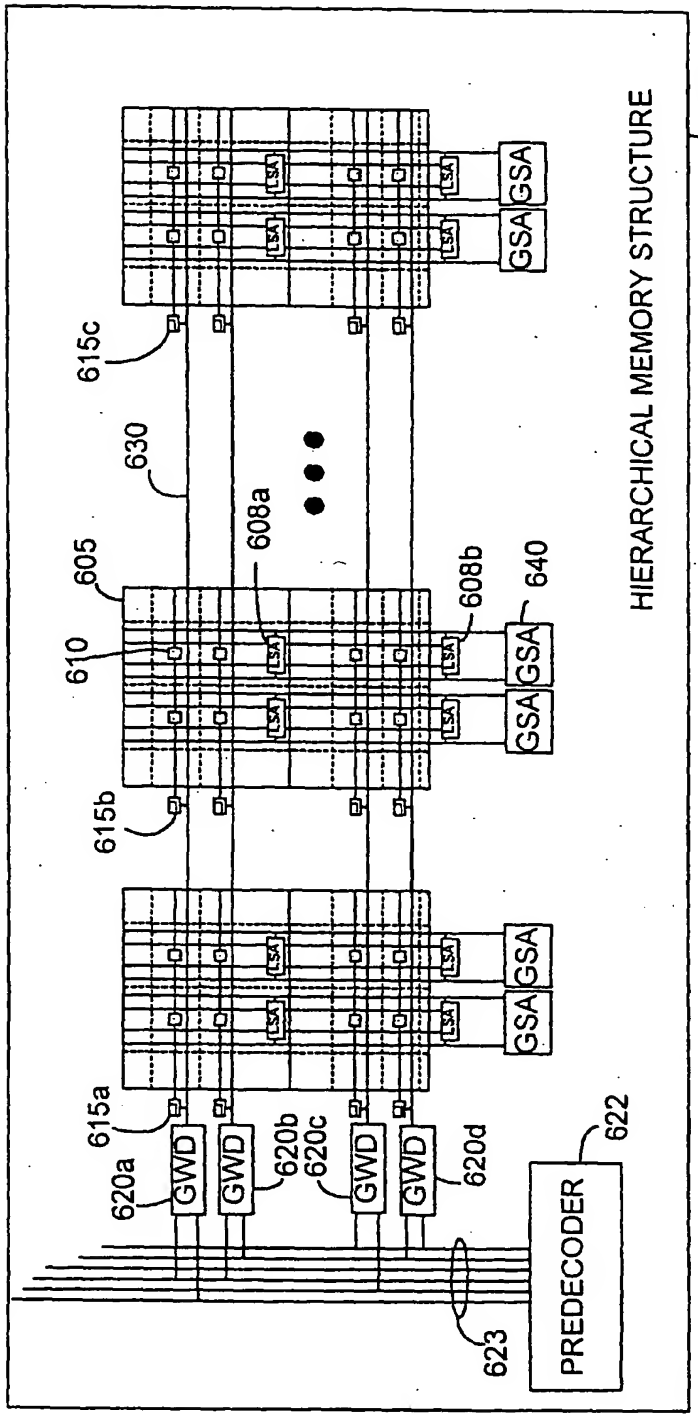
HIERARCHICAL MEMORY STRUCTURE
600
615c
630
608a
605
610
608b
640
615b
615a
620a
620b
620c
620d
622
623
GWD
GSA
LSA
PREDECODER

FIG. 6

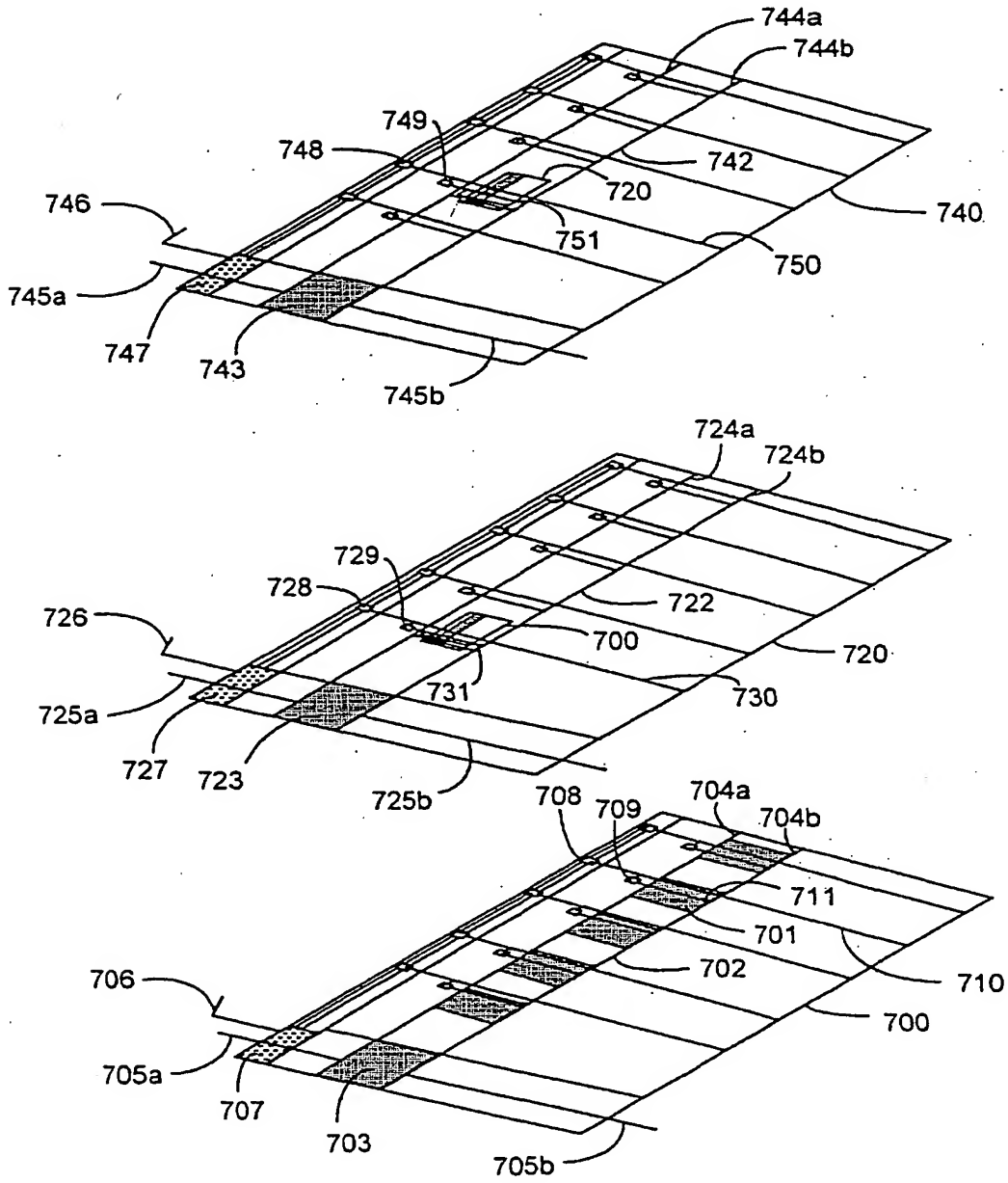
744a
744b
749
748
742
720
746
740
751
750
745a
747
743
745b
724a
724b
729
728
722
726
700
720
731
730
725a
727
723
725b
708
709
704a
704b
711
701
702
706
710
700
705a
707
703
705b

FIG. 7

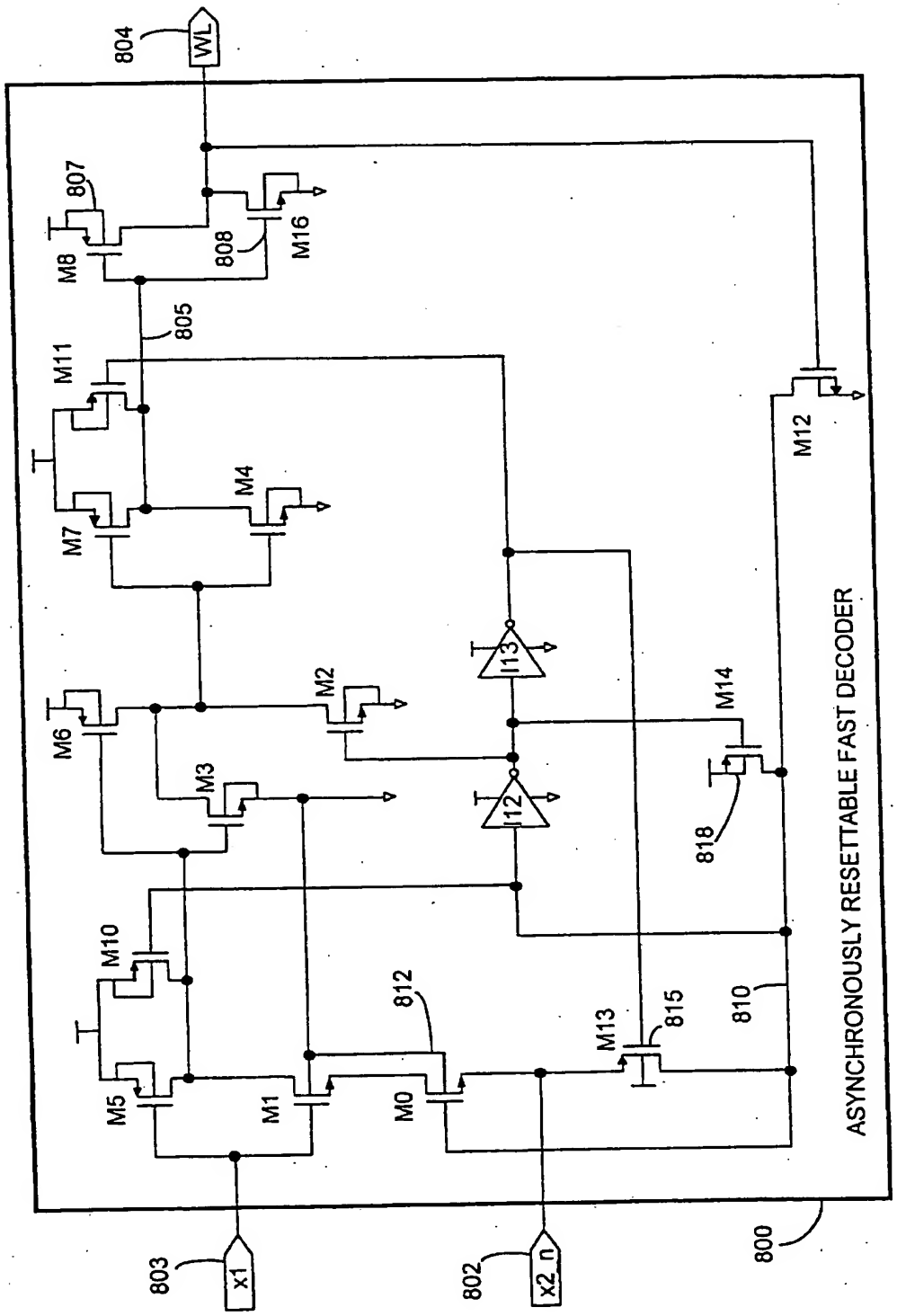
804
WL
807
M8
808
M16
805
M11
M12
M4
M7
M2
M6
M3
I13
I12
M14
818
M10
812
M13
815
810
M5
M1
M0
ASYNCHRONOUSLY RESETTABLE FAST DECODER
800
803
x1
802
x2_n

FIG. 8

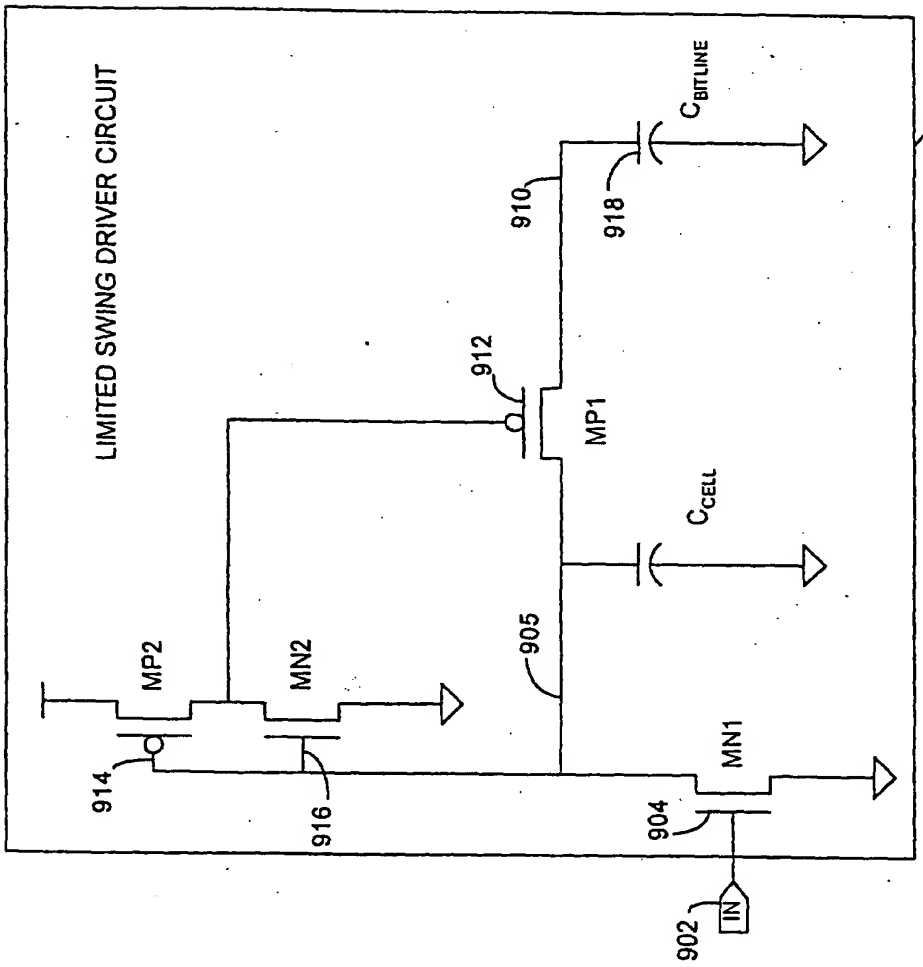
LIMITED SWING DRIVER CIRCUIT
900
$C_{BITLINE}$
910
918
912
MP1
C_{CELL}
905
MP2
MN2
914
916
MN1
904
902
IN

FIG. 9

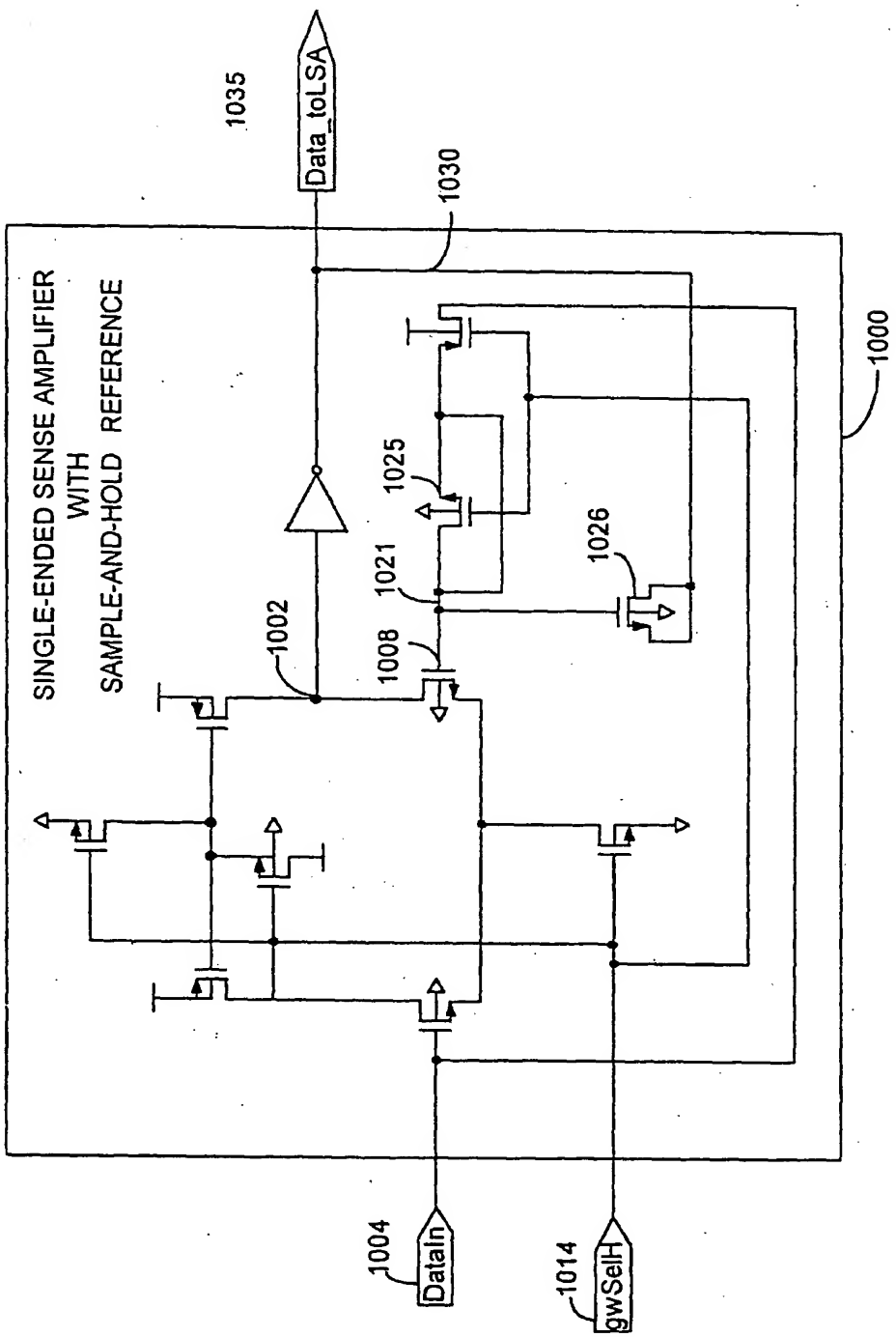
SINGLE-ENDED SENSE AMPLIFIER
WITH
SAMPLE-AND-HOLD REFERENCE
1035
Data_toLSA
1030
1000
1025
1026
1021
1002
1008
1004
DataIn
1014
gwSelH

FIG. 10

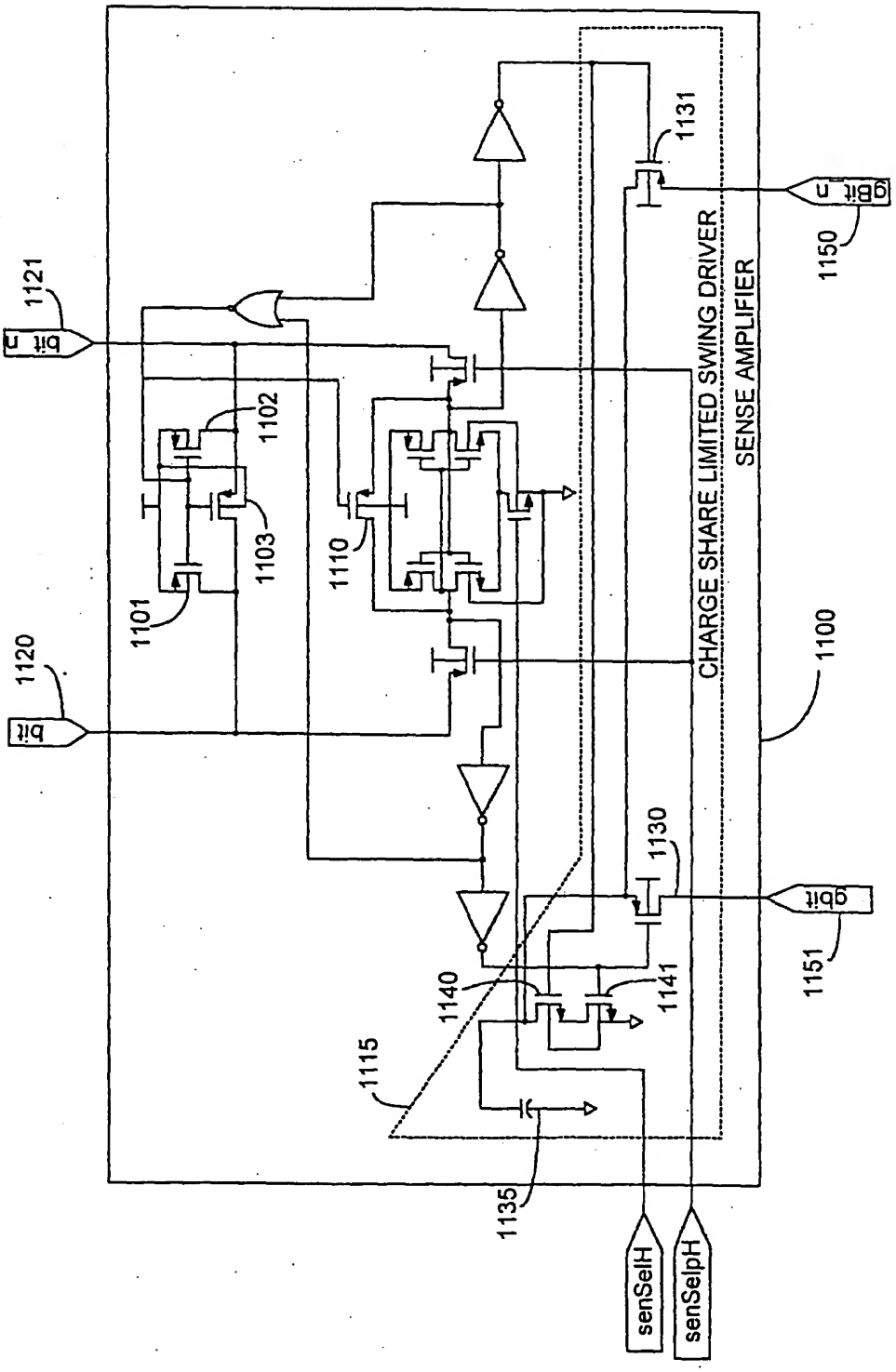
1121
bit n
1120
bit
1101
1102
1103
1110
1131
gBit n
1150
CHARGE SHARE LIMITED SWING DRIVER
SENSE AMPLIFIER
1100
1130
gbit
1151
1140
1141
1115
1135
senSelH
senSelpH

FIG. 11

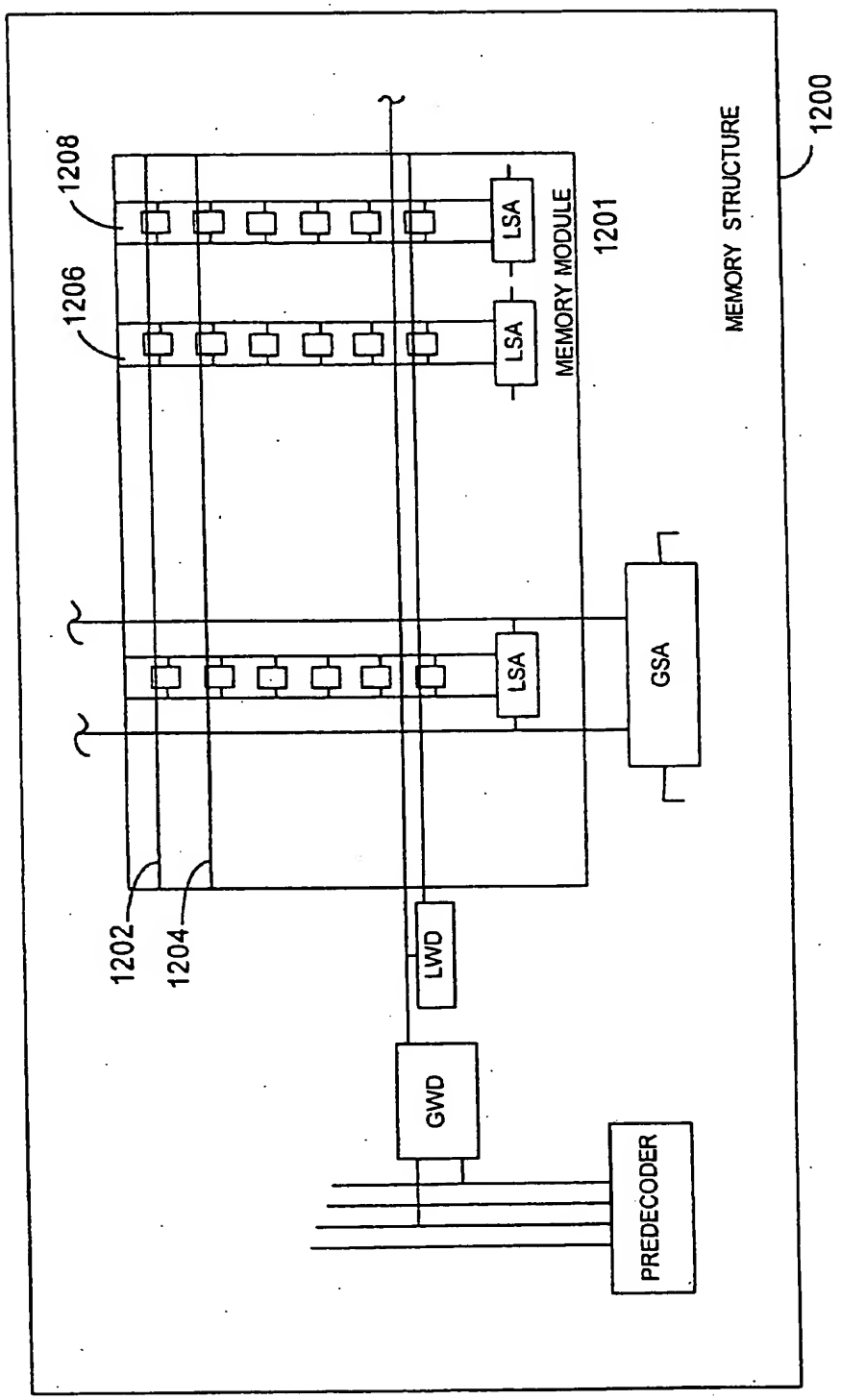
1200
MEMORY STRUCTURE
1201
MEMORY MODULE
1208
1206
LSA
LSA
LSA
GSA
1202
1204
LWD
GWD
PREDECODER

FIG. 12

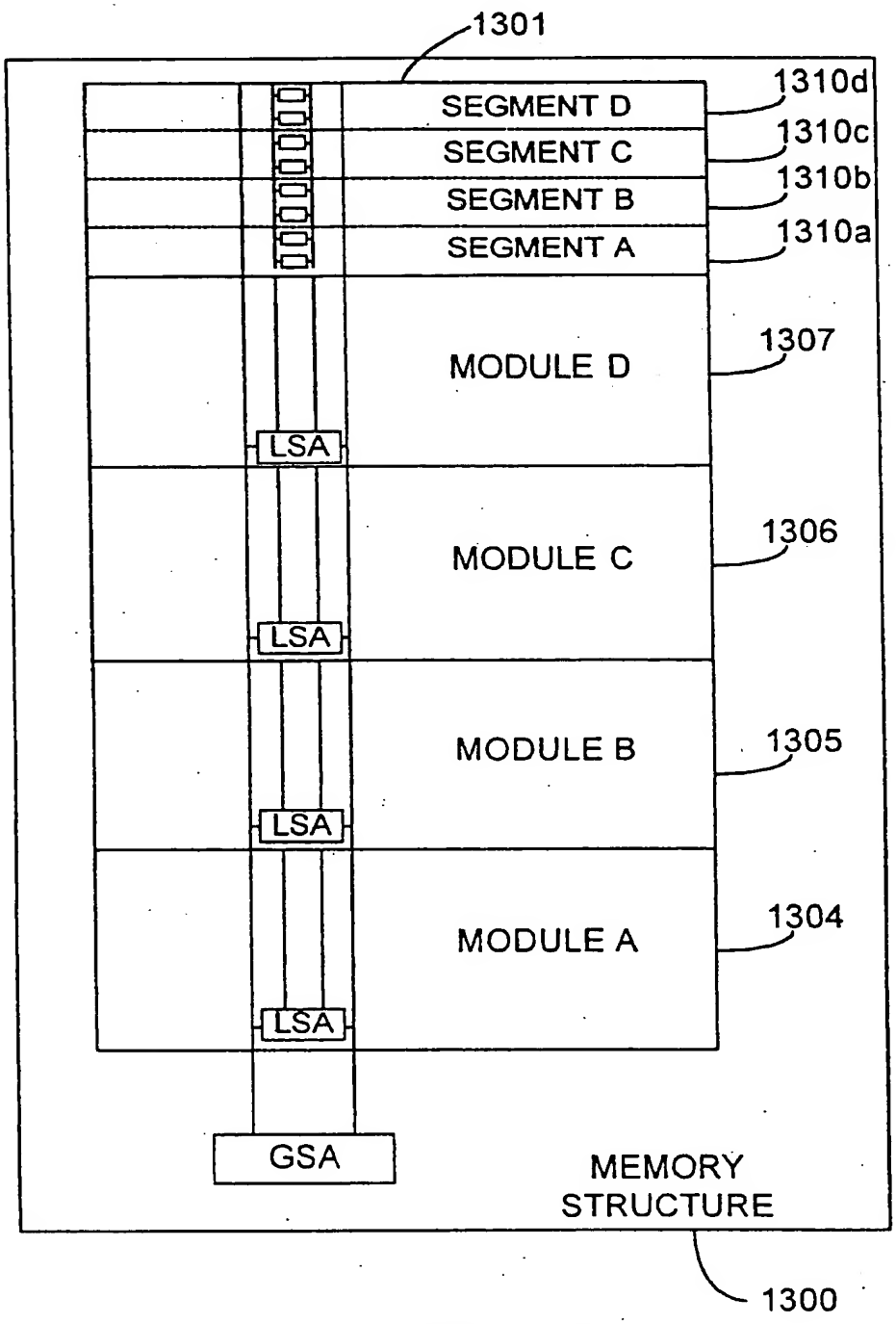
1301
SEGMENT D
SEGMENT C
SEGMENT B
SEGMENT A
1310d
1310c
1310b
1310a
MODULE D
1307
LSA
MODULE C
1306
LSA
MODULE B
1305
LSA
MODULE A
1304
LSA
GSA
MEMORY STRUCTURE
1300

FIG. 13

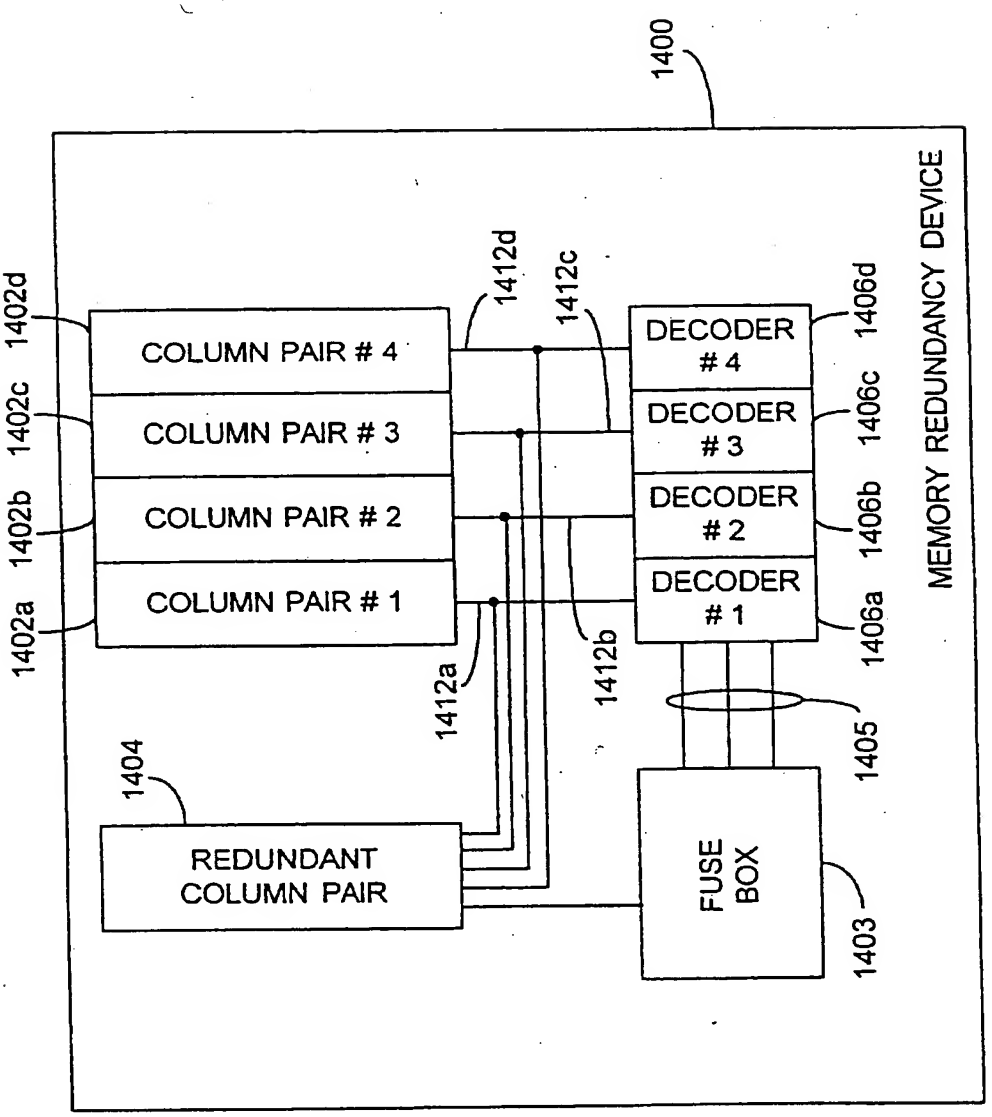
1400
MEMORY REDUNDANCY DEVICE
1402d
1402c
1402b
1402a
COLUMN PAIR # 4
COLUMN PAIR # 3
COLUMN PAIR # 2
COLUMN PAIR # 1
1412d
1412c
1412b
1412a
DECODER # 4
DECODER # 3
DECODER # 2
DECODER # 1
1406d
1406c
1406b
1406a
1405
1404
REDUNDANT COLUMN PAIR
FUSE BOX
1403

FIG. 14

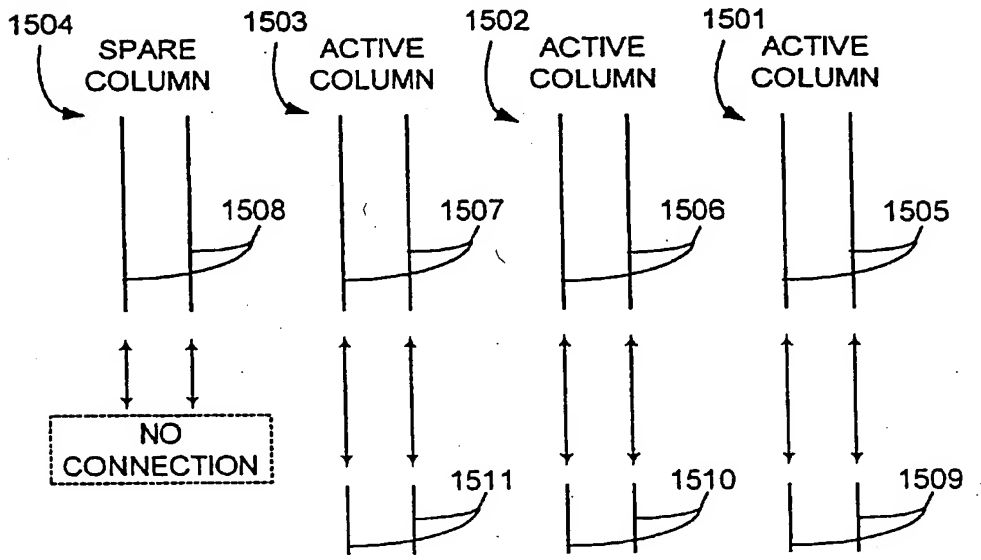

FIG. 15A

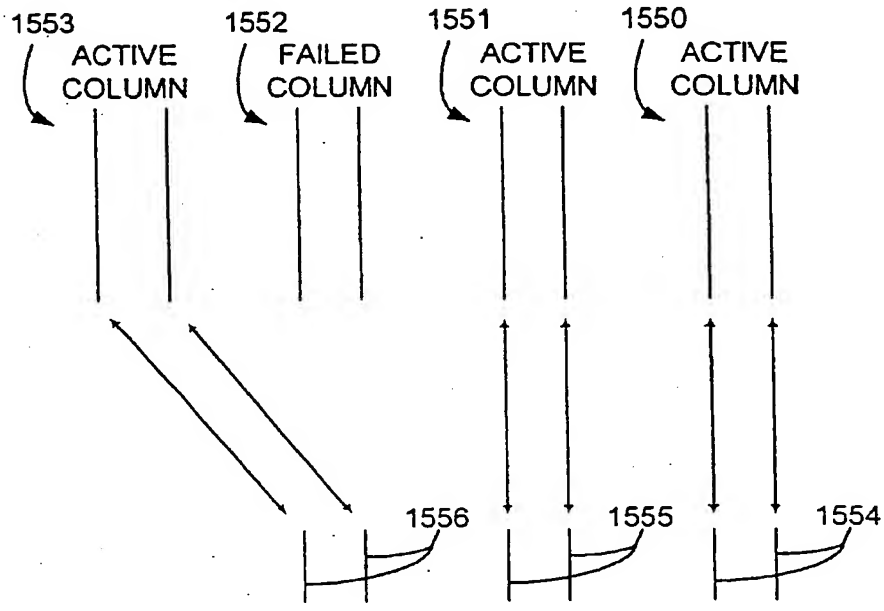

FIG. 15B

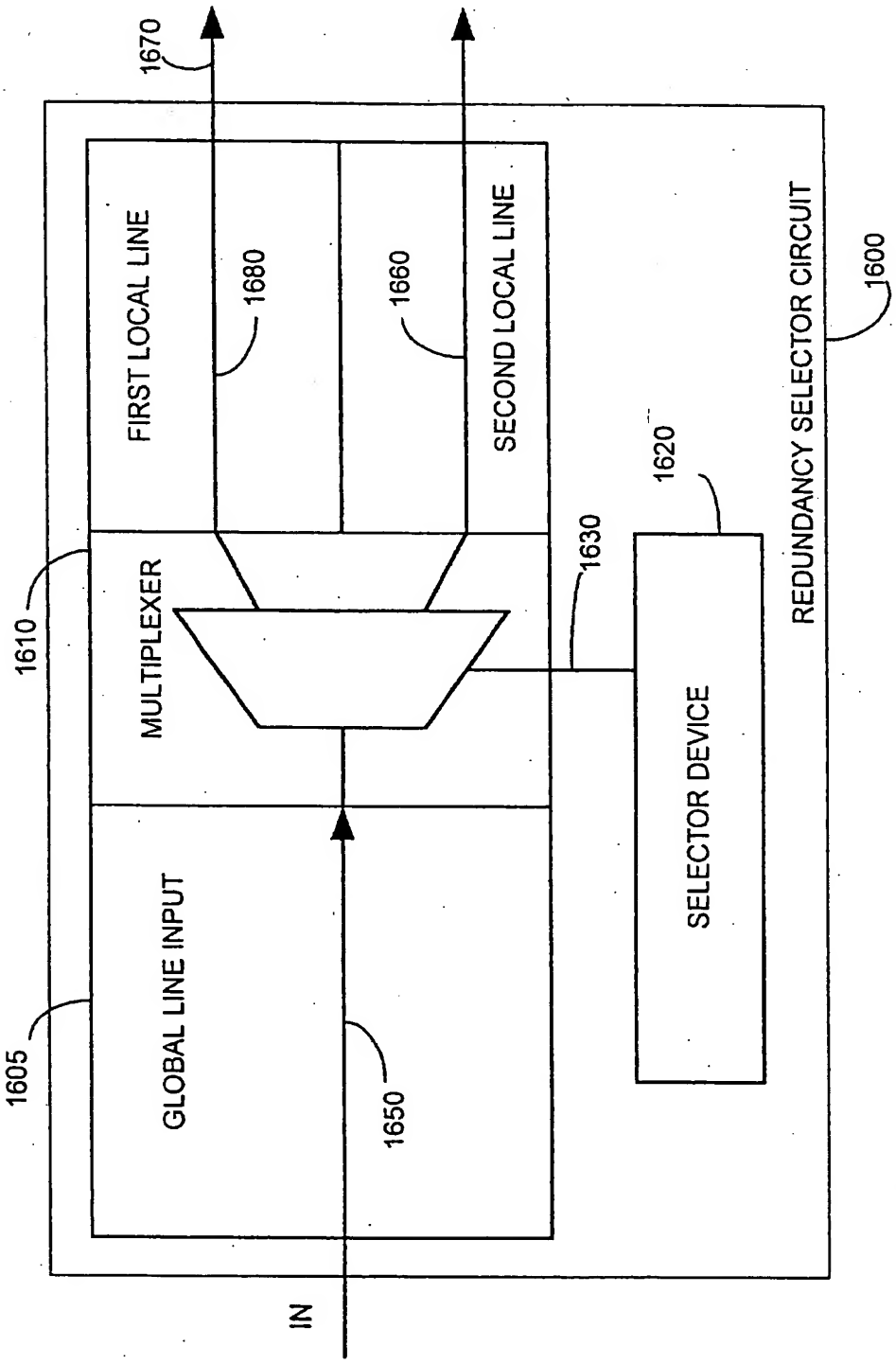
1670
FIRST LOCAL LINE
1680
1660
SECOND LOCAL LINE
REDUNDANCY SELECTOR CIRCUIT
1600
1620
1630
1610
MULTIPLEXER
SELECTOR DEVICE
GLOBAL LINE INPUT
1605
1650
IN

FIG. 16

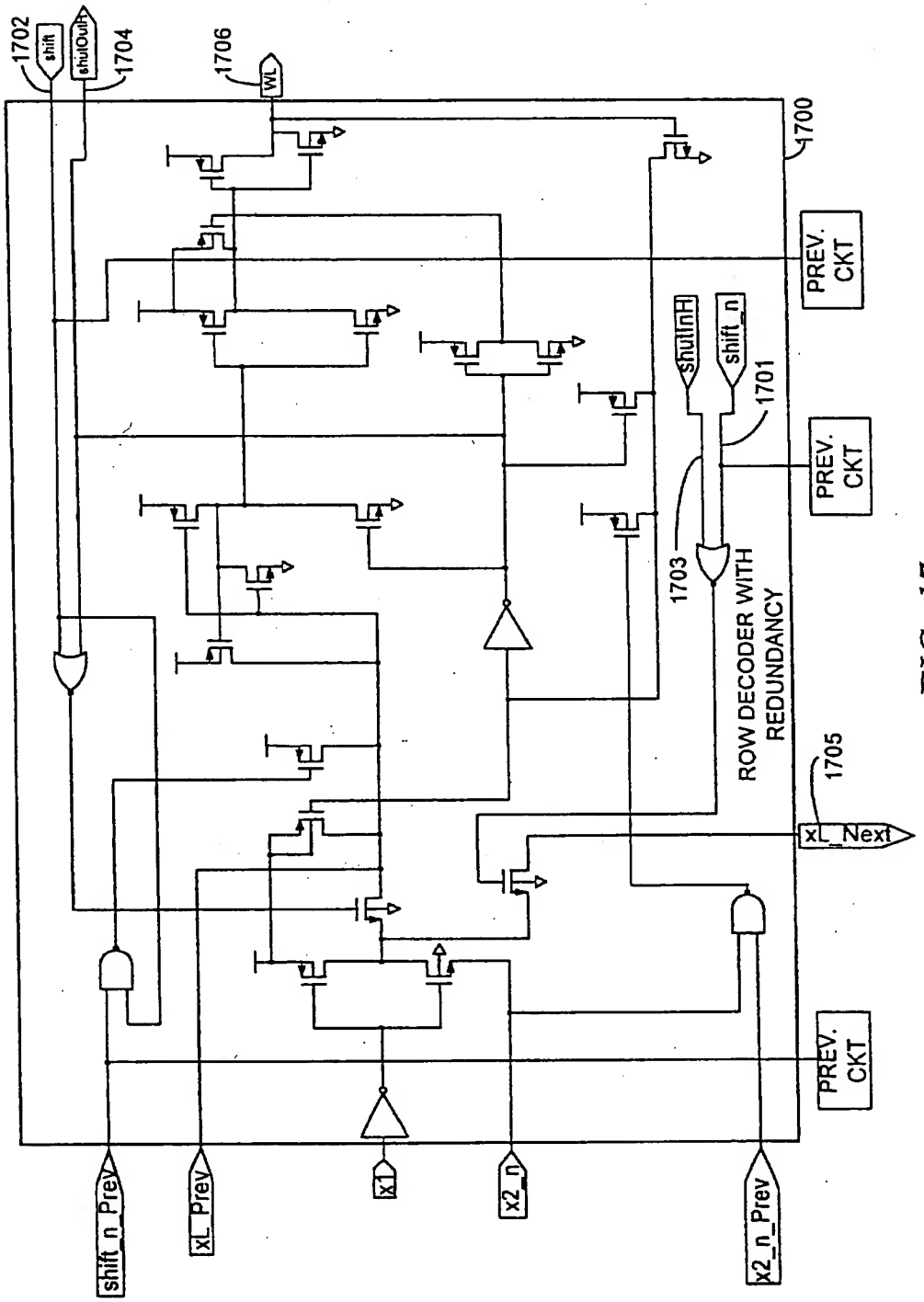
1702
shift
shiftOut
1704
1706
WL
1700
PREV. CKT
shiftH
shift_n
1701
PREV. CKT
1703
ROW DECODER WITH REDUNDANCY
1705
xL_Next
PREV. CKT
shift_n_Prev
xL_Prev
x1
x2_n
x2_n_Prev

FIG. 17

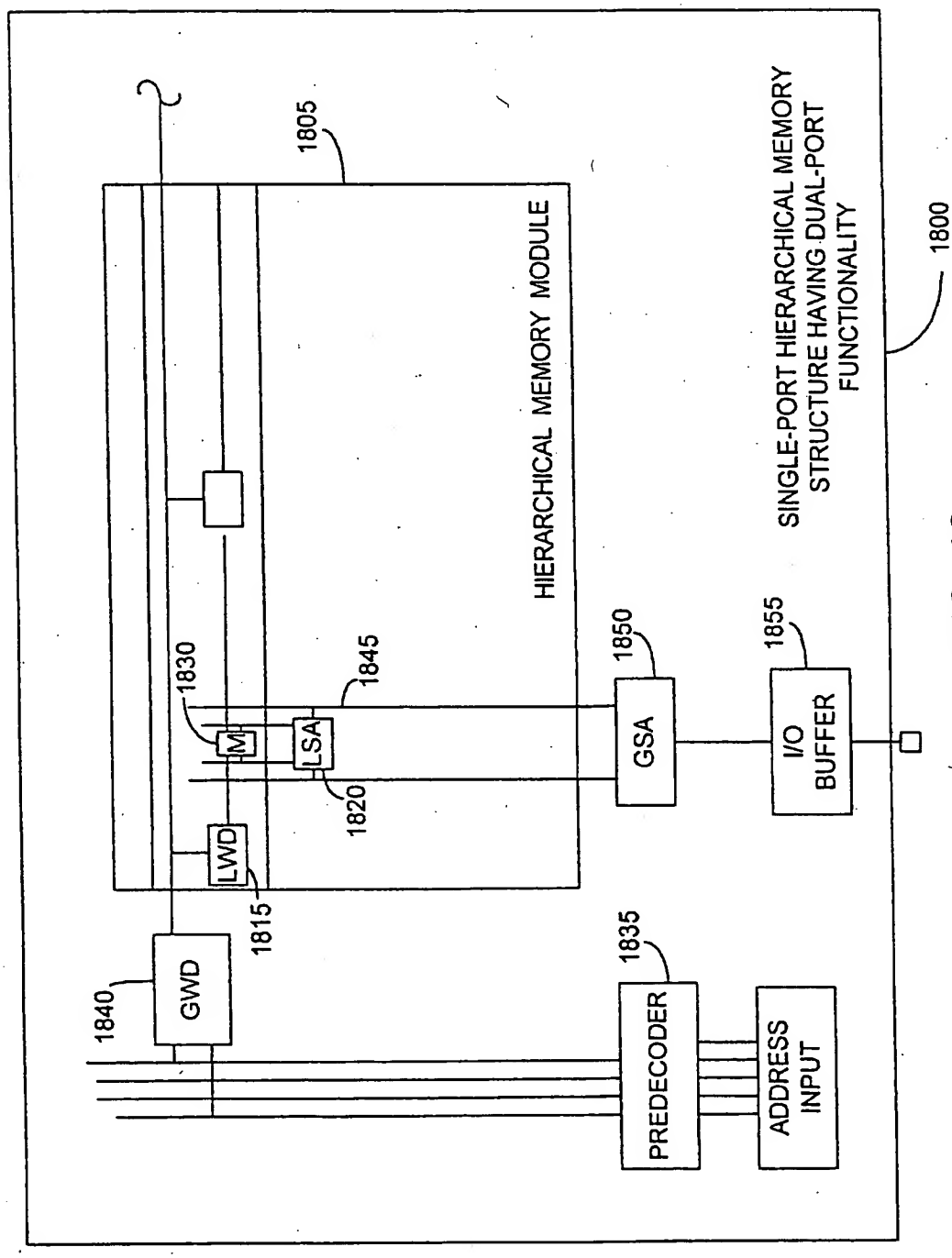
SINGLE-PORT HIERARCHICAL MEMORY STRUCTURE HAVING DUAL-PORT FUNCTIONALITY
1800
HIERARCHICAL MEMORY MODULE
1805
1830
1845
1850
1855
M
LSA
GSA
I/O BUFFER
1820
LWD
1815
1835
1840
GWD
PREDECODER
ADDRESS INPUT

FIG. 18

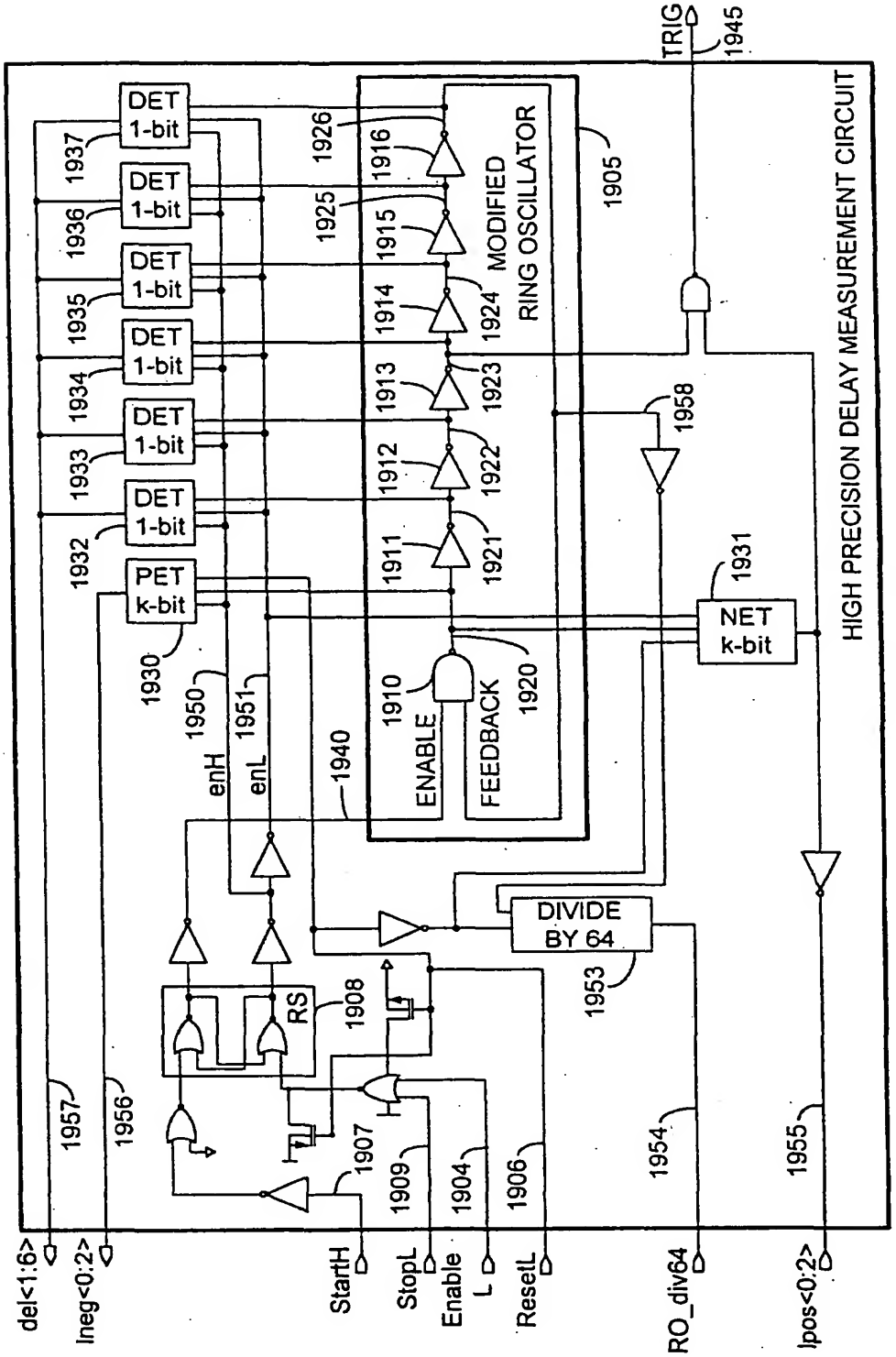
HIGH PRECISION DELAY MEASUREMENT CIRCUIT
TRIG
1945
DET 1-bit
1937
1936
1935
1934
1933
1932
PET k-bit
1930
1926
1925
1916
1915
1914
1913
1912
1911
MODIFIED RING OSCILLATOR
1924
1923
1922
1921
1905
1958
NET k-bit
1931
ENABLE
FEEDBACK
1910
1920
1940
enH
enL
1950
1951
DIVIDE BY 64
1953
RS
1908
1907
1909
1904
1906
1954
1955
1957
1956
del<1:6>
Ineg<0:2>
StartH
StopL
Enable
L
ResetL
RO_div64
Ipos<0:2>

FIG. 19

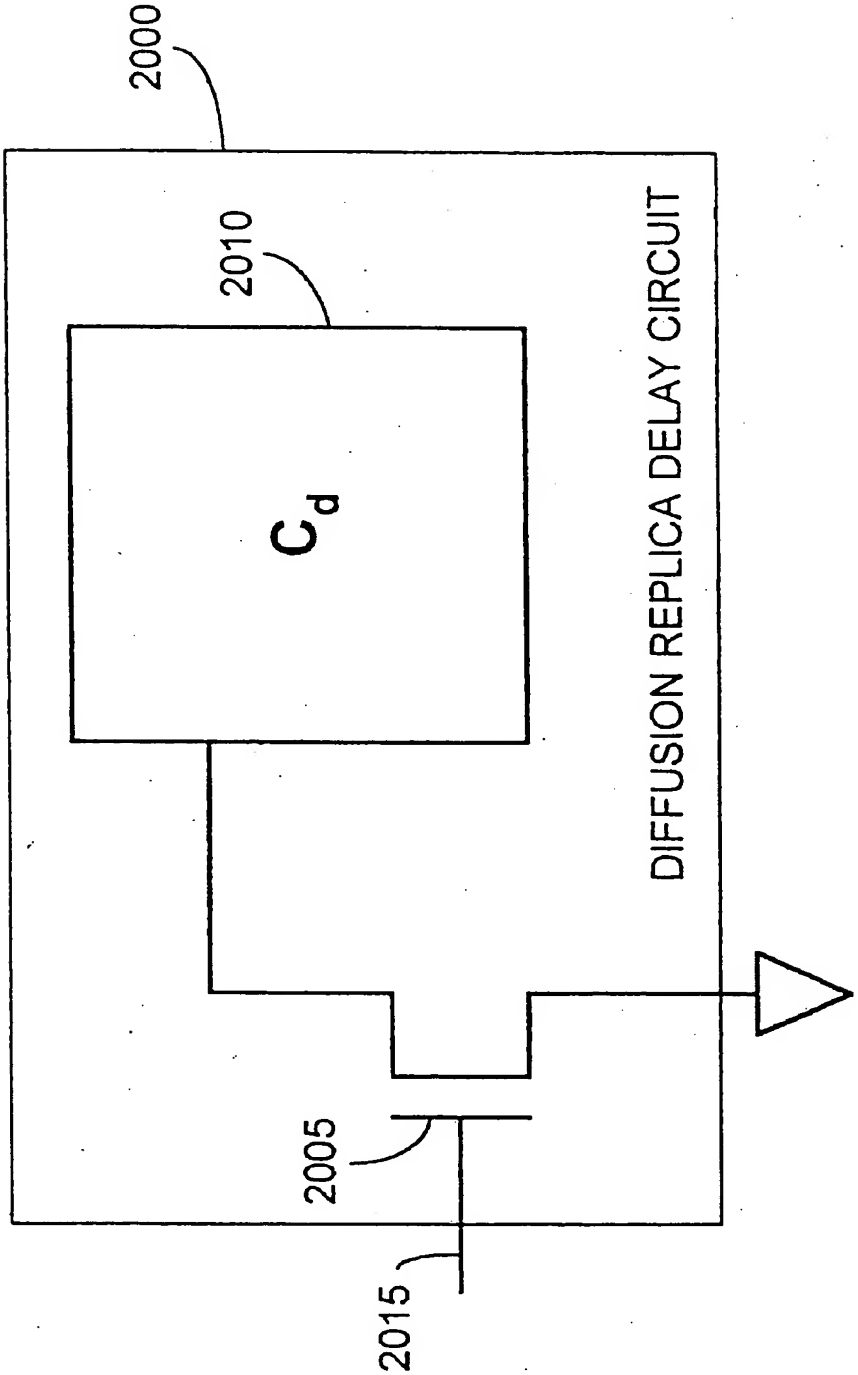

FIG. 20

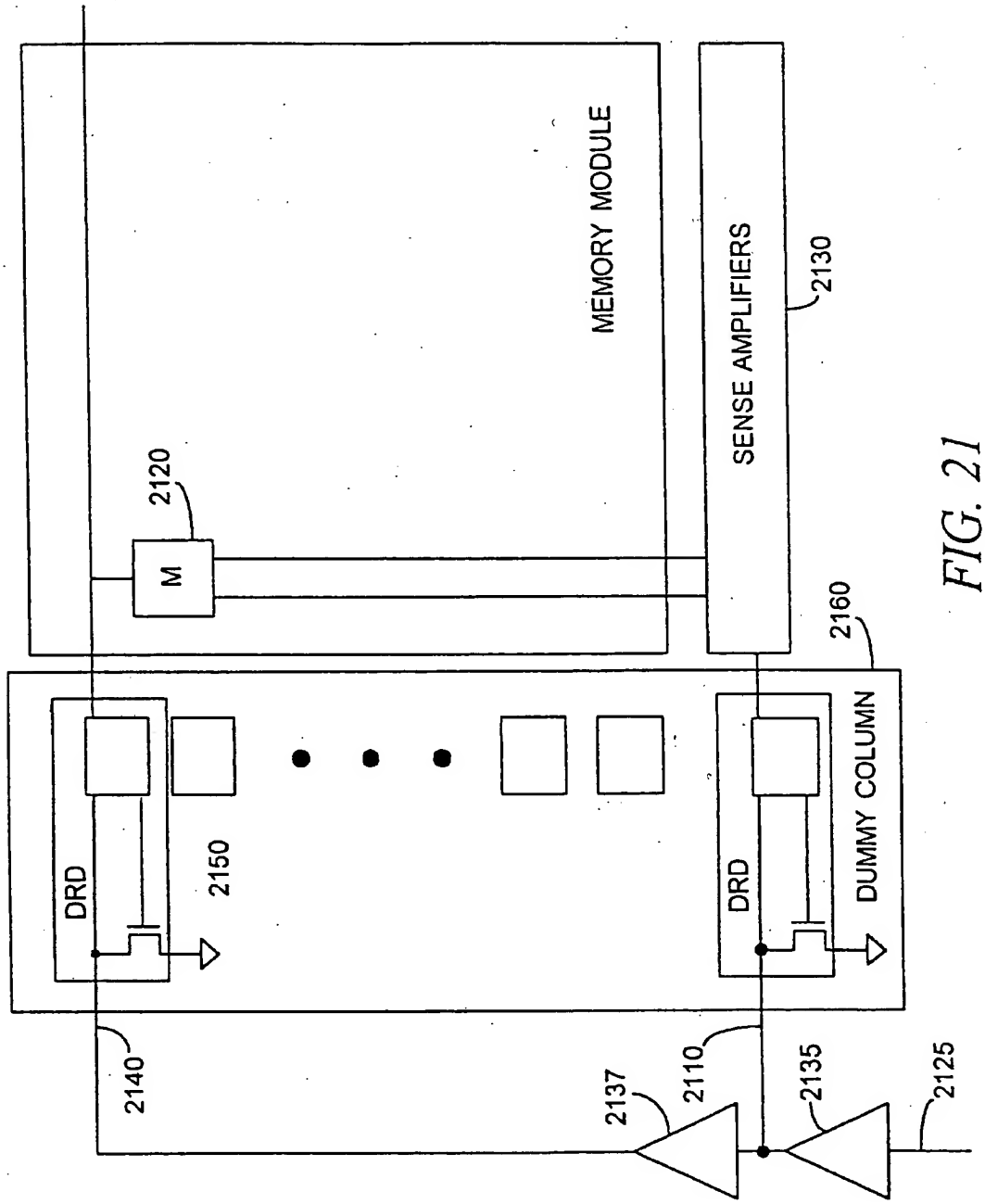
MEMORY MODULE
SENSE AMPLIFIERS
2130
2120
M
2160
DRD
2150
DRD
DUMMY COLUMN
2140
2137
2110
2135
2125

FIG. 21

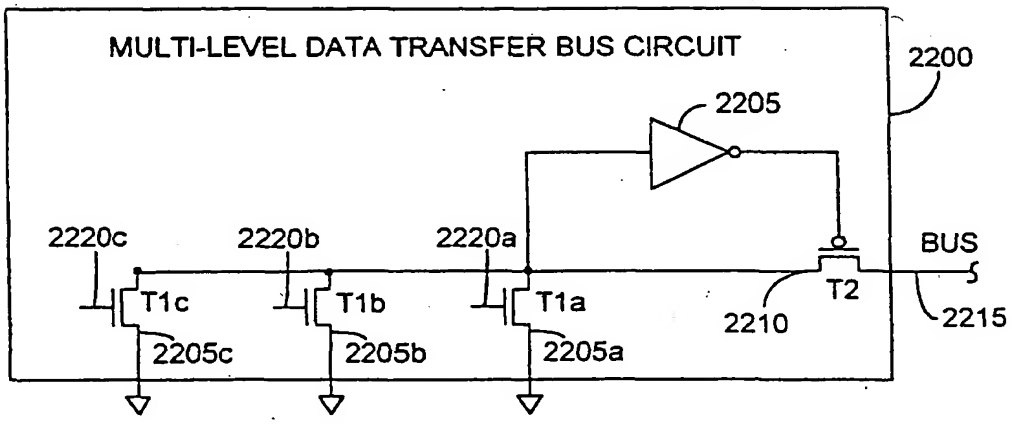

FIG. 22A

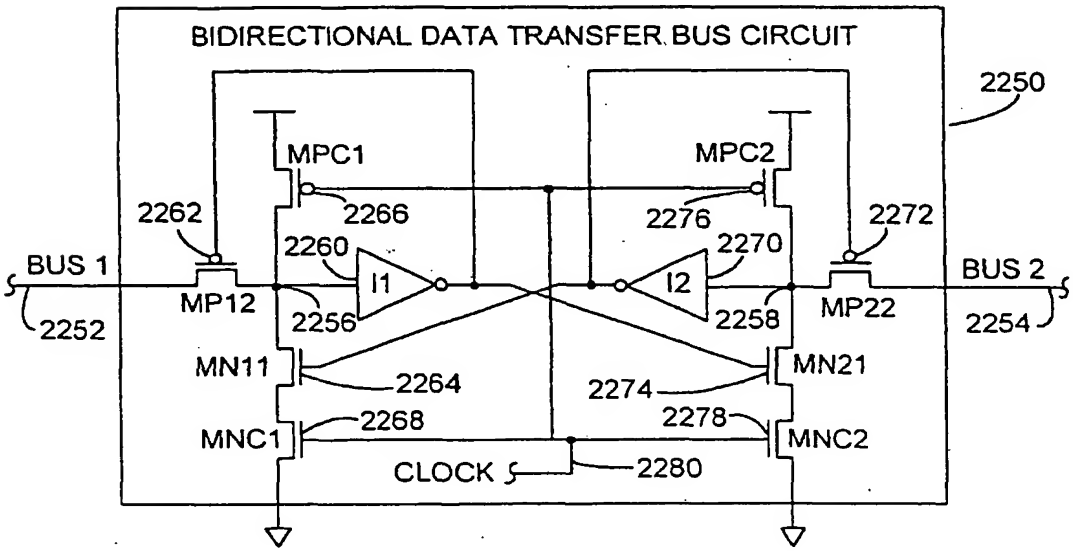

FIG. 22B